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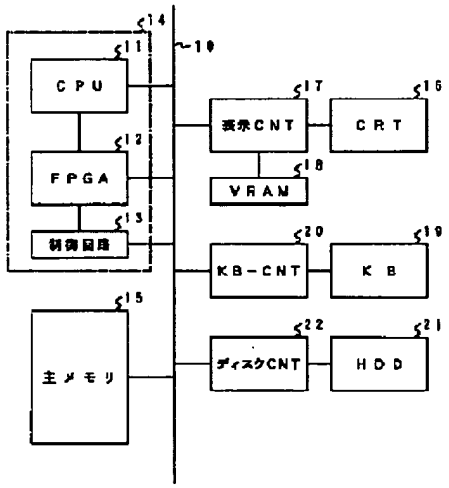
(54) **DATA PROCESSOR**

(57) Abstract:

PURPOSE: To speed up program execution by making a specific part in a program into a hardware macro by a rewritable element with mapping data when the program is started.

CONSTITUTION: A CPU 11, an FPGA 12 which assists the control operation of the CPU 11, a control circuit 13 which controls the writing of mapping data to the FPGA 12, and a main memory 15 are connected to a system bus 10. When the verification of a source program is completed, the part preferably to be made into a hardware macro is analyzed. The specified part is made into the hardware macro matching characteristics of the FPGA 12. Then the block of the specific part made into the hardware macro is divided and mapped corresponding to the circuit scale of the block and FPGA 12 so as to realize the block by the FPGA 12. Further, the remaining module part to be executed by the CPU 11 is compiled into a load module, which is put together with the mapping data to form one access unit, so that access units are stored as series of object programs in a hard disk device 21.



WO 1998010517	A1	EN	55	20		
National Designated States,Original	JP					
Regional Designated States,Original	AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE					
EP 925649	A1	EN			PCT Application	WO 1997US10279
					Based on OPI patent	WO 1998010517
Regional Designated States,Original	DE FR GB					
US 6144220	A	EN			Division of application	US 1996708247
					Division of patent	US 5933023
JP 2001500682	**W**	**JA**	**57**		**PCT Application**	**WO 1997US10279**
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EP 1239592	A2	EN			Division of application	EP 1997929977
					Division of patent	EP 925649
Regional Designated States,Original	DE FR GB					
EP 925649	B1	EN			PCT Application	WO 1997US10279
					Related to application	EP 200211003
					Related to patent	EP 1239592
					Based on OPI patent	WO 1998010517
Regional Designated States,Original	DE FR GB					
DE 69716623	E	DE			Application	EP 1997929977
					PCT Application	WO 1997US10279
					Based on OPI patent	EP 925649
					Based on OPI patent	WO 1998010517

Search result: 1 of 1

(WO/1998/010517) FPGA ARCHITECTURE HAVING RAM BLOCKS WITH PROGRAMMABLE WORD LENGTH AND WIDTH AND DEDICATED ADDRESS AND DATA LINES

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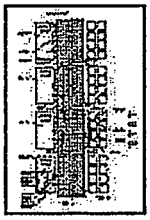
Title: (EN) FPGA ARCHITECTURE HAVING RAM BLOCKS WITH PROGRAMMABLE WORD LENGTH AND WIDTH AND DEDICATED ADDRESS AND DATA LINES
(FR) ARCHITECTURE FPGA A BLOCS DE MEMOIRE RAM POUR LONGUEUR ET LARGEUR DE MOT PROGRAMMABLES ET POUR LIGNES D'ADRESSES ET DE DONNEES SPECIALISEES

Abstract:



(EN) A structure in which blocks of random access memory, or RAM, are integrated with FPGA configurable logic blocks. Routing lines which access configurable logic blocks also access address, data, and control lines in the RAM blocks. Thus, the logic blocks of the FPGA can use these routing lines to access portions of RAM. In one embodiment, dedicated address and data lines access the RAM blocks of the present invention and are connectable to routing lines in the interconnect structure. These lines allow RAM blocks and arrays of RAM blocks to be configured long, wide, or in between, and allow logic blocks to conveniently access RAM blocks in a remote part of the chip. Access to the RAM blocks is efficient in any RAM configuration. Bidirectional buffers or pass devices segment the address and data lines at each RAM block so that a selectable number of RAM blocks can operate together as a RAM. In another embodiment, dedicated data lines are programmably connectable in a staggered arrangement so that RAM blocks can be connected over a long distance without conflict between the RAM blocks.

(FR) La présente invention concerne une structure selon laquelle des blocs de mémoire RAM sont intégrés à des blocs de logiques configurables de FPGA. Les lignes d'acheminement qui donnent accès aux blocs de logiques configurables donnent également accès aux lignes d'adresses, de données et de commande dans les blocs de RAM. Il en résulte que les blocs de logiques de FPGA peuvent se servir de ces lignes d'acheminement pour accéder à des parties de RAM. Selon une réalisation, des lignes d'accès spécialisées pour les adresses et les données assurent l'accès aux blocs de RAM de l'invention, ces lignes pouvant se connecter aux lignes d'acheminement dans la structure d'interconnexion. Ces lignes permettent une configuration en longueur, en largeur, ou intermédiaire, des blocs de RAM et des matrices de blocs de RAM, ce qui permet aux blocs de la logique d'accéder commodément aux blocs de RAM dans une zone éloignée du microcircuit. L'accès aux blocs de RAM reste efficace quelle que soit la configuration de la RAM. Des tampons et des structures de remise bidirectionnels assurent la segmentation des lignes d'adresses et de données au niveau de chaque bloc de RAM de façon que de blocs de RAM en une certaine quantité puissent fonctionner ensemble comme s'ils ne formaient qu'une RAM. Dans le cas d'une autre réalisation, les lignes de données spécialisées sont connectables par programmation selon un agencement faisant que les blocs de RAM sont connectables sur des longues distances sans conflits d'accès entre blocs de RAM.

Designated States: JP.
European Patent Office (EPO) (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE)

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